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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,024	11/16/2000	Masato Mitsuhashi	108066-00018	3168

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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/713,024	MITSUHASHI ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) *1-4 and 6* is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on ____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

JD

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions in view of the amendment dated 8/5/05 is required under 35 U.S.C. 121:

I. Claims 1-4 and 6, drawn to a clock switching circuit structure, classified in class 710, subclass 305.

II. Claims 5 and 7-8, drawn to a processing to control the switching in a circuit, classified in class 710, subclass 104.

2. Inventions I and II are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In the instant case, the Invention II as claimed can be practiced with another materially different produce. Invention II claims receiving means and inhibiting means, which can be practice by any other types of logical gates.

3. Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

4. A telephone call was made to Mr. Sam Huang, the applicant's representative, on August 18, 2005 to request an oral election to the above restriction requirement. Applicant elects the Invention II on August 24, 2005 without traverse. Applicant is advised to cancel the un-elected Invention I when the case is in the condition of allowance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 5 and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Parmenter et al. (U.S. Patent No. 5,679,353).

Referring to claim 5: Parmenter discloses receiving a faster PLL clock signal (figure 2, structuer 19 receives 2X_CLK2), receiving a switch signal for switching an output (figure 2, SR1 issues the controls of the selection), inhibiting outputting clock signal (figure 2, structures 19 and 21 under controls of the SR1), and outputting the PLL clock signal according to the frequency differences (the outputs of 1X_CLK2 and 2X_CLK2). As Applicant pointed out, Parmenter discloses the waiting (Remark, page 10, 2nd paragraph), which is the claimed counting. Hence, claim is anticipated by the Parmenter.

Referring to claims 7-8: Parmenter discloses a PLL circuit (figure 2, structure 15) that generates a fast clock (figure 2, node 2X_CLK2) whose frequency is more than twice as much as a frequency of the basic signal (figure 2, node 17). Parmenter further discloses multiplexers and their associated control means (figure 2, structures 19, 21, and their control means structure SR1), which are equivalent to the claimed inhibiting circuit that inhibits said fast clock by a time (figure 2, the logic circuit node 27, column 2, lines 11-19) when said basic clock disappears in said output in the case of switching said output from said basic clock to the fast clock, or a term which depends on the difference between said frequency of the basic clock and the frequency of

the fast clock in the case of switching. As Applicant pointed out, Parmenter disclsoes multiplexers 19 and 21 switch between the basic clock and faster clock, and the Parmenter shows the locked condition signal PLL LOCK for controlling he multiplexers (Remark, page 10, 2nd paragraph). Therefore, Parmenter's combined structure of structure 15, 21, and SR1 is equivalent to the claimed first circuit, and Parmenter's combined structure of 15, 19, and SR1 is equivalent to the claimed second circuit. Hence, claims are anticipated by the Parmenter.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Yokogawa et al. (U.S. Patent No. 4,872,155) in view of Ishikawa (U.S. Patent No. 6,346,830).

Referring to claim 5: Yokogawa's invention discloses a PLL circuit including a phase comparator comparing two asynchornized clocks' signals (column 4, lines 47-51), and it further discloses that the PLL generates the clock in synchronism (column 5, lines 4-5); thus, Yokogawa

discloses the receiving a PLL clock signal generated from a PLL circuit based on the basic clock signal. Yokogawa further discloses the counting the clock signal number, inhibiting the clock output, and output PLL clock signal after a predetermined number of clock signals (column 4, lines 59-64, column 5, lines 4-6, figure 10). Although Yokogawa discloses the PLL circuit for comparing phases of different clocks' speeds (column 4, lines 47-49), Yokogawa does not explicitly disclose that the PLL clock is faster than the clock speed as the amended claim recites.

Ishikawa discloses an I/O interface with PLL circuits for supporting different I/O clock speeds (figure 5). Ishikawa teaches one to synchronize the clock speed in response to data output and data input with different PLL speeds (column 2, lines 53-67, column 3, lines 1-30). Ishikawa discloses that in order to have a reliable reception of data, it is necessary to establish the value of data at a particular phase of the clock (column 2, lines 29-32), and Ishikawa teaches applying the PLL to synchronize either a faster clock speed or a slower clock speed to establish the value of data at a particular phase of the clock (column 2, lines 53-67, column 3, lines 1-30), which is equivalent to the claimed predetermined number set according to the frequency differences. Since Ishikawa's interface is to connect two devices with two different speeds, and Ishikawa has two separate PLLs for transmitting data at two opposite directions, one of the Ishikawa's PLLs must be faster than the system/reference clock due to the different speeds between the two devices.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Ishikawa's teaching onto Yokogawa because Ishikawa teaches one to establish a reliable data reception by establishing the value of data at a particular phase of the clock with two separate PLLs synchronizing both input data speed and output data speed.

Response to Arguments

10. In response to Applicant's argument that the prior art Parmenter does not discloses the newly amended limitations; and Applicant further argues that Parmenter provides that switching is executed without generating glitches and loss-of-state during the mode transition, therefore, the control of Parmenter waits until the next clock phase boundary to change the clock mode (Remark, page 10, 2nd paragraph): As Applicant pointed out, Parmenter discloses multiplexers 19 and 21 switch between the basic clock and faster clock, and the Parmenter shows the locked condition signal PLL LOCK for controlling he multiplexers (Remark, page 10, 2nd paragraph). Therefore, Parmenter's combined structure of structure 15, 21, and SR1 is equivalent to the claimed first circuit, and Parmenter's combined structure of 15, 19, and SR1 is equivalent to the claimed second circuit. In response to Applicant's argument that Parmenter waits until the next clock phase boundary, Applicant's claims do not include any limitation precluding the alleging waiting practice, and Applicant's claimed invention does not require the elimination of the waiting in order to be functioning.

11. In response to Applicant's argument that the claim 5 is rejected under the 102(b) (Remark, page 10, last paragraph): The claim 5 is rejected under 103(a) as indicated by the leading paragraphs 6 and 7 in Office Action dated 3/7/05. The 102(b) stated in paragraph 8 is a typo, and the amended claim 5 is considered accordingly above.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on max flex. If attempts to reach the examiner by telephone

are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
September 1, 2005

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